Amendments to the Specification:

Please amend the paragraph starting on page 5, line 4 as follows:

In the multi-chip memory device of Fig. 5, the first lead frame **54-1** of the upper chip **52-1** and the first lead frame [[**54-2**]] **54-3** of the lower chip **52-2** are connected to each other, and the second lead frame **54-2** of the upper chip **52-1** and the second lead frame **54-4** of the lower chip **52-2** are also connected to each other. The lead frames **54-1** to **54-4** are connected to a plurality of control signal applying pins of the upper and lower chips **52-1** and **52-2**, respectively. The lead frames connected to a plurality of data input/output pins of the chips **52-1** and **52-2** are not connected to each other and are configured independent of each other. In other words, all first and second lead frames of the chips **52-1** and **52-2** except the lead frames connected to the data input/output pins of the chips **52-1** and **52-2** of 32M×8 bits are connected to each other, respectively. As a result, the multi-chip memory device has the same pin configuration as shown in Fig. 3. The first and second lead frames **54-1** and **54-2** of Fig. 5 are used as signal input/output pins.

Please amend the paragraph starting on page 6, line 2 as follows:

The memory devices **12-1** to **12-4** arranged in a dotted line portion **10'** are mounted on the front surface **10** of the memory module. Operation of the memory devices [[**12-3**]] **12-1** and [[**12-4**]] **12-2** is enabled in response to the chip select signal (CSB0), and the system clock signal (CLK0) is enabled in response to the clock enable signal (CKE0), so that data of 32 bits is input or output in response to the system clock signal (CLK0). Also, operation of the memory devices [[**12-1**]] **12-3** and [[**12-2**]] **12-4** is enabled in response to the chip select signal ~~(CSB1)~~ (CSB0), and the system clock signal (CLK1) is enabled in response to the clock enable signal ~~(CKE1)~~ (CKE0), so that data of 32 bits is input or output in response to the system clock signal (CLK1). That is, the memory devices **12-1** to **12-4** are enabled in response to the chip select signal (CSB0) and the clock enable signal (CKE0) and input or output data of 64 bits in response to the system clock signal (CLK0, CLK1).

Please amend the paragraph starting on page 6, line 14 as follows:

The memory devices **22-1** to **22-4** arranged in a dotted line portion **20'** are mounted on the rear surface **20** of the memory module. Operation of the memory devices **22-1** and **22-2** is enabled in response to the chip select signal (CSB1), and the system clock signal (CLK0) is enabled in response to the clock enable signal (CKE1), so that data of 32 bits is input or output in response to the system clock signal (CLK0). Also, operation of the memory devices **22-3** and **22-4** are enabled in response to the chip select signal (CSB1), and the system clock signal (CLK1) is enabled in response to the clock enable signal (CKE1), so that data of 32 bits input or output in response to the system clock signal (CLK1). That is, the memory devices [[**12-1**]] **22-1** to [[**12-4**]] **22-4** are enabled in response to the chip select signal (CSB1) and the clock enable signal (CKE1) and input or output data of 64 bits in response to the system clock signal (CLK0, CLK1).

Please amend the paragraph starting on page 6, line 26 as follows:

However, as described above, conventional memory devices may [[be]] have degraded performance due to heat that may be generated when the two chips perform an input/output of data at the same time.